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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,974	01/15/2004	Jenoe Tihanyi	1890-0033	4260

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 07/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/757,974	TIHANYI, JENOE	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 28 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claims 28 and 29, the recitation " the first MOS transistor and the second MOS transistor constitute compensation components" is indefinite because it is not clear as to the first and the second MOS transistors are compensation components of the MOSFET circuit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foreign Application (JP 6-53 800) in view of Kimura (USP. 6,851,849), Hartwick (USP. 4,881,024), Kumar (USP. 6,855, 981) and Pavlin (USP. 5,438,286)

Regarding claims 15, 16 and 17, figure 3 of JP 6-5380 show a MOSFET circuit comprising: a first MOS transistor (Q2), a second transistor (Q4) coupled in parallel with the first MOS transistor, a constant voltage element is a zener diode (SBD2). Figure 3 of the foreign application does not show that the first MOS transistor has a first number of cells and the second MOS transistor has a second number of cells. Figure 2 of Pavlin shows a MOSFET circuit comprising first second MOS transistor (TP1) and second NMOS transistor

(TP2) coupled in parallel. The second transistor (TP2) has a second number of cells less (10-40 times) than the first number of cells (col. 4, lines 35-40) for providing a circuit having low threshold current that is many times lower than the circuit of the foreign application wherein the transistors have an equal number of cells. (col. 4, lines 50-62). Therefore, it would have been obvious to an artisan having skills in the art to replace the transistors of the foreign application with the transistors taught by Pavlin for providing a circuit having low threshold current that is many times lower than circuit wherein the transistors have an equal number of cells. The resistor is element (R2).

Regarding claims 18 and 19, figure 3 of the foreign application does not show that there is a resistor coupled in series with the zener diode. Figure 1 of Hartwick shows a resistor (R1) coupled in series with the zener diode for limiting the current flowing through the diode. Therefore, it would have been obvious to an artisan having skills in the art to implement a resistor in series with the diode (SBD2) for limiting the current flowing through the diode.

Regarding claim 20, figure 6 of Kimura shows that the zener diode (30) and the resistor (40b) are integrated with one another for having a compact circuit.

Regarding claims 21, 22, 23 and 32, the technique of fabrication of the zener diode and the resistor are well known in the art and is fully shown by Kumar (6,855, 981, col. 11, lines 24-30). Kumar does not show that "the dope concentration of the highly doped layer is less than 10exp 19 charge carrier cm –exp 3". However, it is old and well known and it would have been an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative predetermined value of a differential input voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative predetermined value of a differential input voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is

critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III). Therefore, it would have been obvious to one having ordinary skill in the art to select the dope concentration of the highly doped layer to be less than 10exp 19 charge carrier cm –exp 3" dependent upon particular environment of use to ensure optimum performance.

Regarding claims 24, figure 3 of JP 6-5380 show a MOSFET circuit comprising: a first MOS transistor (Q2), a second transistor (Q4) coupled in parallel with the first MOS transistor, a constant voltage element is a zener diode (SBD2). Figure 3 of the foreign application does not show that the first MOS transistor has a first number of cells and the second MOS transistor has a second number of cells. Figure 2 of Pavlin shows a MOSFET circuit comprising first second MOS transistor (TP1) and second NMOS transistor (TP2) coupled in parallel. The second transistor (TP2) has a second number of cells less (10-40 times) than the first number of cells (col. 4, lines 35-40) for providing a circuit having low threshold current that is many times lower than the circuit of the foreign application wherein the transistors have an equal number of cells. (col. 4, lines 50-62). Therefore, it would have been obvious to an artisan having skills in the art to replace the transistors of the foreign application with the transistors taught by Pavlin for providing a circuit having low threshold current that is many times lower than circuit wherein the transistors have an equal number of cells. The resistor is element (R2).

Regarding claims 25-27 and 29, the first number of cells is 10 to 40 times larger than the second number of cells (col. 4, lines 35-40). The first number of cells is from 15,000 to 20,000 (col. 4, lines 38-40).

Regarding claim 28, transistors (TP1) and (TP2) of Pavlin constitute a main composite transistor (TP) that is used to compensate the threshold current by lowering it X times lower (col. 4, lines 50-62).

Regarding claims 30, figure 3 of "JP6-53800" show a MOSFET circuit comprising: a first MOS transistor (Q2), a second transistor (Q4) coupled in parallel with the first MOS transistor, a constant voltage element is a zener diode.
Figure 3 of the foreign application does not show that the first MOS transistor has a first number of cells and the second MOS transistor has a second number of cells. Figure 2 of Pavlin shows a MOSFET circuit comprising first second MOS transistor (TP1) and second NMOS transistor (TP2) coupled in parallel. The second transistor (TP2) has a second number of cells less (10-40 times) than the first number of cells (col. 4, lines 35-40) for providing a circuit having low threshold current that is many times lower than the circuit of the foreign application wherein the transistors have an equal number of cells. (col. 4, lines 50-62). Therefore, it would have been obvious to an artisan having skills in the art to replace the transistors of the foreign application with the transistors taught by Pavlin for providing a circuit having low threshold current that is many times lower than circuit wherein the transistors have an equal number of cells. The resistor is element (R2). Even though, "JP 6-5380" does not mention that the zener diode is fabricated with a technique recited in claim 30. However, this technique is a common technique shown in US Pat. 6,855,981, col. 11, lines 23-44.

Regarding claim 31, the resistor is element (R2). Kuma col. 11 shows that the resistor can be formed by the pn junction between the polycrystalline layer and the zone.

Regarding claims 33 and 34, the first number of cells is 10 to 40 times larger than the second number of cells (col. 4, lines 35-40). The first number of cells is from 15,000 to 20,000 (col. 4, lines 38-40).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
07-25-05

TUAN T. LAM
PRIMARY EXAMINER